REMARKS

These Remarks are in reply to the Office Action mailed October 5, 2009. Claims 1-26 were pending in the Application prior to the outstanding Office Action. Claims 3 is current being amended, and no claims are currently being canceled or added, leaving claims 1-26 for the Examiner's consideration. In view of the above amendments and the remarks below, Applicants respectfully request that the rejections be reconsidered and withdrawn, and that a Notice of Allowance be issued.

I. Allowable Subject Matter

Applicants thank the Examiner for indicating that claims 5-7, 17-19, 22 and 23 are allowed. Applicants also thank the Examiner for indicating that claims 3, 4, 21, 24 and 26 (which were objected to as being dependent upon a rejected base claim) would be allowable if rewritten in independent form including the limitations of the base claim and any intervening claim. **Claim 3** has been rewritten to be in independent form, including the limitations of its base claim. Accordingly, Applicants respectfully request that claim 3 be allowed. Claim 4 depends from claim 3, and thus, should also be allowed.

II. Summary of Rejections

Claims 1, 2, 8, 10-16, 20 and 25 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over U.S. Publication No. 2002/0122518 to Yasuda et al. (hereafter "Yasuda") in view of U.S. Patent No. 7,099,426 to Cory et al. (hereafter "Cory"). Claim 9 was rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Yasuda and Cory as applied to Claim 8, and further in view of U.S. Patent No. 7,302,396 to Cooke (hereafter "Cooke").

III. Discussion of the Claims

Claim 1

In claim 1, each of a plurality of audio amplifier channels includes "a buffer management unit ... configured to control a rate at which samples are read from the input buffer to achieve a target difference between the values of the read and write pointers".

Claim 1 requires that "for a first one of the channels, the target difference comprises a predetermined value". For an example, assume that the "predetermined value" = 100.

Claim 1 also requires that "for the remainder of the channels, the target difference comprises the actual difference between the values of the read and write pointers of the first one of the channels."

The tables shown below provide an example of how the system of claim 1 would operate at three exemplary points in time (i.e., time 1, time 2 and time 3).

time 1

	Ch. 1 (master)	Ch. 2 (slave)	Ch. 3 (slave)
Actual Difference b/w R and W pointers	105	102	107
Target Difference	100	105	105

time 2

	Ch. 1 (master)	Ch. 2 (slave)	Ch. 3 (slave)
Actual Difference b/w R and W pointers	104	101	106
Target Difference	100	104	104

time 3

	Ch. 1 (master)	Ch. 2 (slave)	Ch. 3 (slave)
Actual Difference b/w R and W pointers	103	99	100
Target Difference	100	103	103

At "time 1", the actual difference between the read (R) and write (W) pointers in the three channels are different, as shown above. For the first channel (assumed to be Ch. 1), the target difference is the predetermined value (100 in this example), regardless of the actual difference (i.e., 105). For the remainder of the channels (Ch. 2 and Ch. 3), the target difference is the actual difference between the values of the read and write pointers of the Ch. 1 (105 in this example), regardless of the actual difference between the read and write pointers within Ch. 2 and Ch. 3.

At "time 2", the actual difference between the read (R) and write (W) pointers in three channels are again different, as shown above. For Ch. 1, the target difference is again the predetermined value (100 in this example), regardless of the actual difference (i.e., 104). For the remainder of the channels (Ch. 2 and Ch. 3), the target difference is the actual difference between the values of the read and write pointers of the Ch. 1 (104 in this example), regardless of the actual difference between the read and write pointers within Ch. 2 and Ch. 3.

At "time 3", the actual difference between the read (R) and write (W) pointers of the three channels are again different, as shown above. For Ch. 1, the target difference is again the predetermined value (100 in this example), regardless of the actual difference (i.e., 103). For the remainder of the channels (Ch. 2 and Ch. 3), the target difference is the actual difference between the values of the read and write pointers of the Ch. 1 (103 in this example), regardless of the actual difference between the read and write pointers within Ch. 2 and Ch. 3.

It was asserted in the Office Action that Yesuda teaches that a target difference for a master channel is a predetermined difference.

Further, it was asserted in the Office Action that Cory teaches that slave channels are synchronized to a master channel, "and that synchronization steps read on a target difference being an

actual difference for the remainder of the channels." It is unclear what is meant by "and that synchronization steps read on a target difference being an actual difference for the remainder of the channels," but it is presumed that this is an assertion that Cory teaches that for the slave channels, the target difference comprises the actual difference between the values of the read and write pointers of the master channel. Applicants respectfully disagree, as explained below.

Specifically, it was asserted in the Office Action that column 3, line 66 – column 5, line 14 of Cory teaches "alignment blocks or sequences to match the separate channels", and therefore, "Cory is teaching synchronizing slave channel buffers to a master channel buffer". For arguments sake, Applicants will presume that Cory does teach that slave channel buffers are synchronized to a master channel buffer. However, this does not mean that Cory is synchronizes the slave channel buffers to the master channel buffer in the same manner as is done in claim 1. As mentioned above, claim 1 requires that "for the remainder of the channels [presumably the slave channels], the target difference comprises the actual difference between the values of the read and write pointers of the first one of the channels [presumably the master channel]." As shown in the example described above, this means that the "target difference" for the slave channels will depend entirely on the actual difference between the values of the read and write pointers of the master channel, and will not depend on the actual difference between the read and write pointers in the slave channels. Nothing in column 3, line 66 – column 5, line 14 of Cory teaches these specific limitations of claim 1. Accordingly, a prima facie case of obviousness has not been established. If the Examiner is to maintain this rejection, Applicants respectfully request that the Examiner explain in additional detail how Cory is being interpreted to teach these limitations of claim 1.

In the second to last sentence on page 4 of the Office Action, it was alleged that column 29, lines 56-66 teaches "controlling the read pointers of slave buffers based on the actual difference in the master buffer". As was explained in the Applicants' remarks filed on September 4, 2009, this portion of Cory (i.e., Column 29, lines 56-66) explains that the master elastic buffer can maintain data alignment for all the slave elastic buffers and itself by means of a clock correction signal (CC_enb), a channel bonding signal (CB_load), a stagger control signal (STAG), and an address increment signal (incr_addr). In other words, this section of Cory merely explains that the master elastic buffer can control itself and the slave buffers by controlling clocks, by channel bonding, by staggering and/or by incrementing addresses. However, this portion of Cory, and other portions of Cory, do not teach or suggest that the rate at which samples are read from the input buffers of the remainder of the channels (presumably the slave channels) is controlled specifically to achieve the actual difference between the values of the read and write pointers of the first one of the channels (presumably the master channel). If the Examiner is to maintain this assertion, Applicants respectfully request that the Examiner explain in additional detail how Cory is being interpreted to teach these limitations of claim 1.

In column 3, line 66-column 5, line 14, Cory teaches that "alignment sequences" consisting of one or more "alignment blocks" are used to correlate the data blocks stored in different elastic buffers. This portion of Cory also explains that the master elastic buffer must control the clock correction operations for all the slave elastic buffers. However, this portion of Cory certainly does not teach or suggest that "for the remainder of the channels [presumably the slave channels], the target difference comprises the actual difference between the values of the read and write pointers of the first one of the channels [presumably the master channel]", as required by claim 1.

For at least the reasons set forth above, Applicants respectfully assert that the cited references, alone or in combination, do not teach or suggest that "for a first one of the channels, the target difference comprises a predetermined value" and that "**for the remainder of the channels, the target difference comprises the actual difference between the values of the read and write pointers of the first one of the channels.**" Accordingly, Applicants respectfully request that the 103(a) rejection of claim 1 be reconsidered and withdrawn.

Claims 2, 20 and 21

Claims 2, 20 and 21 depend from and add additional features to independent claim 1. Applicants assert that these claims are patentable over the cited references for at least the reason that they depend from claim 1, as well as for the features that they add.

Claims 8-13 and 24

For at least similar reasons to those discussed above with regards to claim 1, Applicants assert that independent claim 8 is patentable over the applied references. Claims 9-13 and 24 depend from and add additional features to independent claim 8. Applicants assert that these claims are patentable over the cited references for at least the reason that they depend from claim 8, as well as for the features that they add.

Claims 14, 25 and 26

For at least similar reasons to those discussed above with regards to claim 1, Applicants assert that independent claim 14 is patentable over the applied references. Claims 25 and 26 depend from and add additional features to independent claim 14. Applicants assert that these claims are patentable over the cited references for at least the reason that they depend from claim 14, as well as for the features that they add.

Claims 15 and 16

For at least similar reasons to those discussed above with regards to claim 1, Applicants assert that independent claim 15 is patentable over the applied references. Claims 25 and 26 depend from and add additional features to independent claim 14. Applicants assert that these claims are patentable over the cited references for at least the reason that they depend from claim 14, as well as for the features that they add.

Claims 17-19

For at least similar reasons to those discussed above with regards to claim 1, Applicants assert that independent claim 17 is patentable over the applied references. Claims 18 and 19 depend from and add additional features to independent claim 17. Applicants assert that these claims are patentable over the cited references for at least the reason that they depend from claim 17, as well as for the features that they add.

IV. Conclusion

For at least the reasons specified above, Applicants respectfully assert that the claims as amended are still patentable, and another Notice of Allowance is respectfully requested.

The Examiner is respectfully requested to telephone the undersigned if he can assist in any way in expediting issuance of a patent.

The Commissioner is authorized to charge the required fees and any underpayment of fees or credit any overpayment to Deposit Account No. 06-1325 for any matter in connection with this reply, including any fee for extension of time, which may be required.

Respectfully submitted,

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